Full translation of Japanese laid open patent 10-270445
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CLAIMS

[Claim(s)]

[Claim 1] The semiconductor device characterized by providing the following. Semiconductor substrate. An insulating layer including the 1st which is formed on the aforementioned semiconductor substrate and has the front face of the same level mostly, and 2nd fields. The high density wiring group which is formed on the field of the above 1st and includes many circuit patterns of the 1st height and the 1st width of face. The single dummy circuit pattern which is formed on the field of the above 2nd and has latus width of face rather than the 1st height of the above, the same height, and the 1st width of face of the above, The layer insulation layer which covers the aforementioned high density wiring group and a dummy circuit pattern, is formed, and has the front face of the same level mostly on the above 1st and the 2nd field, The 1st upper circuit pattern which is formed on the layer insulation layer on the field of the above 1st, and includes two or more circuit patterns, It is formed on the layer insulation layer on the field of the above 2nd, has width of face narrower than the aforementioned dummy circuit pattern, and is the single 2nd upper circuit pattern of the cross direction of a dummy circuit pattern mostly arranged along a center.

[Claim 2] The semiconductor device according to claim 1 with which the aforementioned layer insulation layer has a low front face rather than the aforementioned simultaneously same level in the field between the above 1st and the 2nd field.

[Claim 3] The semiconductor device according to claim 1 or 2 with which the aforementioned layer insulation layer includes the field formed by SOG.

[Claim 4] The manufacture method of a semiconductor device of having wiring of multilayer structure including the dummy wiring which is characterized by providing the following and which does not contribute to the connection state of a circuit element. a) The process for which the relation between the width of face of the isolated lower layer wiring and the layer insulation layer thickness which has the flattening function formed on it is prepared beforehand. b) The process for which the measurement result which formed the circuit pattern which crowded in the 1st field on a semiconductor substrate, formed on it the layer insulation layer which has a flattening function, and measured the thickness of a layer insulation film beforehand is prepared. c) The process which asks for the width of face of a request of the dummy wiring arranged under the upper wiring isolated from the aforementioned relation and the aforementioned measurement result. d) While forming the lower layer wiring which crowded in the 1st field on a semiconductor substrate The

process which forms the lower layer wiring which has the width of face of the above-mentioned request only in the part in which the upper wiring of the 2nd field in which isolated wiring is formed as upper wiring is formed as dummy wiring, e) Process which forms the upper wiring in the process which forms the layer insulation film which covers the aforementioned lower layer wiring and has a flattening function, and the 1st field of f above and the 2nd field.

[Claim 5] The manufacture method of the semiconductor device according to claim 4 which forms dummy wiring in the space between all wiring which has the width of face beyond a predetermined value in the 1st field of the above in the aforementioned processes b and d.

[Claim 6] The manufacture method of a semiconductor device including the sub process in which the aforementioned process e forms a conformal insulator layer, and the sub process which forms an SOG film on it according to claim 4 or 5.

[Claim 7] The semiconductor device characterized by providing the following. Semiconductor substrate. An insulating layer including the 1st which is formed on the aforementioned semiconductor substrate and has the front face of the same level mostly, and 2nd fields. The high density wiring group which is formed on the field of the above 1st and includes many circuit patterns of the 1st height and the 1st width of face. The dummy circuit pattern group which is formed on the field of the above 2nd and has latus width of face rather than the 1st width of face of the above as a whole with the 1st height of the above, and the same height, The layer insulation layer which covers the aforementioned high density wiring group and a dummy circuit pattern group, is formed, and has the front face of the same level mostly on the above 1st and the 2nd field, The 1st upper circuit pattern which is formed on the layer insulation layer on the field of the above 1st, and includes two or more circuit patterns, It is formed on the layer insulation layer on the field of the above 2nd, has width of face narrower than the aforementioned dummy circuit pattern group, and is the single 2nd upper circuit pattern of the cross direction of a dummy circuit pattern group mostly arranged along a center.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention relates to the semiconductor device which has a multilayer interconnection including dummy wiring about a semiconductor device and its manufacture method, and its manufacture method.

[0002]

[Description of the Prior Art] In a semiconductor integrated circuit, wiring is complicated with improvement in a degree of integration, and a multilayer interconnection becomes indispensable. In order to insulate between two or more wiring layers, a layer insulation layer is used. A layer insulation layer also performs

the insulation between the circuit patterns from which it differs in the same wiring layer.

[0003] Although the silicon-oxide layer formed by chemistry gaseous-phase deposition (CVD) has the outstanding dielectric property, it is a conformal layer which has surface morphology which imitated the ground configuration. If a layer insulation layer is formed only by the conformal insulating layer, a surface level difference will also become large with the increase in the number of layers of a multilayer interconnection, and problems, such as an open circuit and short-circuit, will also be produced.

[0004] In order to carry out flattening of the front face of a layer insulation layer, the method of using the insulating layer which has flattening properties, such as spin-on glass (SOG) and a silicon-oxide layer by TEOS(tetrapod ethoxy silane)-ozone, is proposed. Although the insulating layer which has these flattening properties cancels the irregularity on the front face of a ground to some extent, it has left technical problems, like it is difficult to carry out flattening of the latus crevice of width of face to the same extent as the crevice where width of face is narrow.

[0005] To the latus crevice of width of face, the method of extinguishing the latus crevice of width of face using the circuit pattern which does not contribute to circuit connection of a semiconductor integrated circuit, i.e., a dummy pattern, is learned. For example, in the wiring channel field of a gate array, the method (JP,5-275531,A) of cutting virtual complete wiring according to the circuit connection which arranges wiring and is realized to all fields, the method (JP,1-239873,A) of forming a dummy pattern in the field by which lower layer wiring does not exist in the field in which the upper wiring is formed, etc. are once proposed virtually.

[0006]

[Problem(s) to be Solved by the Invention] In order to form a dummy circuit pattern, the same preparation as the usual circuit pattern formation is required. For example, if it is going to form a dummy circuit pattern in all the fields as for which the semiconductor chip is vacant, the amount of data of a circuit pattern will increase no less than 20 to 30 times. Thus, when it is going to process the immense amount of data, a data processor is also enlarged and it is necessary to apply to processing for a long time.

[0007] The purpose of this invention is offering the semiconductor device which has the multilayer interconnection which can be realized by the few amount of data and can form the upper wiring on an insulating-layer front face flat in efficiency.

[0008] Other purposes of this invention are offering the manufacture method of a semiconductor device of having such a multilayer interconnection.

[0009]

[Means for Solving the Problem] According to one viewpoint of this invention, it is the manufacture method of a semiconductor device of having wiring of multilayer structure including the dummy wiring which does not contribute to the connection state of a circuit element. a) The process for which the relation between the width of face of the isolated lower layer wiring and the thickness of the insulator layer which

has the flattening function formed on it is prepared beforehand, b) The process for which the measurement result which formed the circuit pattern which crowded in the 1st field on a semiconductor substrate, formed on it the layer insulation film which has a flattening function, and measured the thickness of a layer insulation film beforehand is prepared, c) While forming the lower layer wiring which crowded in the process which asks for the width of face of a request of the dummy wiring arranged under the upper wiring isolated from the aforementioned relation and the aforementioned measurement result, and the 1st field on d semiconductor substrate The process which forms the lower layer wiring which has the width of face of the above-mentioned request only in the part in which the upper wiring of the 2nd field in which isolated wiring is formed as upper wiring is formed as dummy wiring, e) The manufacture method of a semiconductor device of having the process which forms the upper wiring in the process which forms the layer insulation film which covers the aforementioned lower layer wiring and has a flattening function, and the 1st field of f above and the 2nd field is offered.

[0010] An insulating layer including the 1st which according to other viewpoints of this invention is formed on a semiconductor substrate and the aforementioned semiconductor substrate, and has the front face of the same level mostly, and 2nd fields, The high density wiring group which is formed on the field of the above 1st and includes many circuit patterns of the 1st height and the 1st width of face, The single dummy circuit pattern which is formed on the field of the above 2nd and has the width of face more than the double precision of the 1st height of the above, the same height, and the 1st width of face of the above, The layer insulation film which covers the aforementioned high density wiring group and a dummy circuit pattern, is formed, and has the front face of the same level mostly on the above 1st and the 2nd field, The 1st upper circuit pattern which is formed on the layer insulation film on the field of the above 1st, and includes two or more circuit patterns, The semiconductor device which is formed on the layer insulation film on the field of the above 2nd, has width of face narrower than the aforementioned dummy circuit pattern, and has the single 2nd upper circuit pattern of the cross direction of a dummy circuit pattern mostly arranged along a center is offered.

[0011] It has the property of the layer insulation film which has a flattening function tending to collect in the field to which wiring crowded, and being hard to collect in the field to which wiring was isolated. Even if it makes the upper isolated wiring correspond and arranges the dummy of the same wiring width of face as isolated wiring in a lower layer, the level difference of a layer insulation layer will arise in a high density field and an isolated wiring field. If the level difference of a layer insulation layer becomes more than the depth of focus grade of an aligner, or it, the precision of phot lithography will fall.

[0012] If the width of face of the lower layer dummy wiring arranged under the isolated upper wiring is increased, the layer insulation layer thickness which collects on it according to the width of face of lower layer dummy wiring will increase. It becomes possible to adjust mostly the front face of the layer insulation layer under

wiring to the same level by measuring beforehand the layer insulation layer thickness which has a flattening function in the high density field of wiring, and choosing the width of face of the lower layer dummy wiring arranged under the upper isolated wiring so that it may correspond to this thickness.

[0013]

[Embodiments of the Invention] this invention person considered arranging lower layer dummy wiring only under the upper wiring in the isolated field in which it is not crowded with wiring in order to cut down the amount of data for dummy wiring formation.

[0014] With reference to drawing 5 , the lower layer wiring 12 and 13 is formed on the ground insulating layer 11 which has a flat front face. The lower layer wiring 12 is a high density circuit pattern currently formed in the high density field RA where wiring crowded. On the other hand, the lower layer dummy wiring 13 is a dummy circuit pattern which is arranged only under the upper wiring 16 and has the same width of face as the upper wiring 16 in the isolated field in which it is not crowded with wiring.

[0015] In addition, in this specification, as for a high density field, the space between the both sides of wiring is a less than 3-micrometer field, and the space between the both sides of wiring of an isolated field is a field 3 micrometers or more.

[0016] The lower layer wiring 12 and 13 is covered and the layer insulation layer 14 which consists of a laminating of silicon-oxide layer 14c by silicon-oxide layer 14a by CVD, silicon-oxide layer 14b by SOG, and CVD is formed. The silicon-oxide layers 14a and 14c by CVD have uniform thickness in all fields mostly. Silicon-oxide layer 14b by SOG absorbs the level difference of a ground, and forms the smooth front face by which flattening was carried out locally. in the high density field RA, the silicon-oxide layer by SOG is formed on the lower layer wiring 12 at the thickness of about 1 law

[0017] In the isolated field RB in which it is not crowded with wiring, even if the lower layer dummy wiring 13 is arranged, the silicon-oxide layer by SOG which collects on it will be thin, and the front face of different level from the front face of the SOG silicon-oxide layer in a high density field will be formed. A level difference d will arise between the front face of the layer insulation layer 14 in the high density field RA, and the front face of the layer insulation layer 14 in the isolated field RB. For this reason, the phot lithography precision at the time of forming the upper wiring 15 and 16 will fall.

[0018] If the field which does not need to arrange dummy wiring in the field in which the upper wiring is not formed, and arranges dummy wiring is restricted only to the field in which the upper wiring is formed, the amount of data for dummy wiring formation is reducible. However, if dummy wiring is used as the same pattern as the upper wiring, the effect of dummy wiring will decrease remarkably.

[0019] Based on the trial result explained above, this invention person proposes adjusting the width of face of lower layer dummy wiring.

[0020] Drawing 1 is the graph and outline cross section showing roughly the flow

chart which shows roughly the manufacture method of the semiconductor device by the example of this invention, and the technical content in each step.

[0021] It asks for the relation between the width of face of lower layer dummy wiring, and the thickness of the layer insulation film which has the flattening function prepared on it in Step S1. The layer insulation film which has a flattening function has the inclination for the thickness H to increase according to the lower layer dummy wiring width of face W, as shown in step S1 right-hand side.

[0022] Formation of the layer insulation film which has a flattening function on certain conditions obtains the layer insulation thickness H according to the wiring width of face W of lower layer wiring in the isolated lower layer wiring top. In advance of manufacture of an actual semiconductor device, such a relation is prepared beforehand. It is desirable to prepare two or more relations according to the formation conditions of a layer insulation layer.

[0023] One of the concrete examples of Step S1 is shown in drawing 2 . As shown in drawing, the lower layer circuit pattern 13 to which width of face W was isolated is formed on the front face of the lower layer insulating layer 11, and the layer insulation layer 14 is formed on it. the 1st silicon-oxide layer 14 according [the layer insulation layer 14] to CVD -- the silicon-oxide layer 14 by a and SOG -- it considers as the laminated structure of 2nd silicon-oxide layer 14c by b and CVD

[0024] The silicon-oxide layers 14a and 14 by CVD are mostly formed in a ground front face conformal one, and do not call at a place, but have the almost same thickness t1 and t2. Silicon-oxide layer 14b by SOG has thickness h depending on the ground configuration. If the formation conditions of a layer insulation layer are fixed, t1 and t2 will take constant value, and only h will change according to a ground configuration.

[0025] Here, the thickness of silicon-oxide layer 14b by SOG in a center section of a circuit pattern 13 is mostly measured as h. it measures how the width of face W of a circuit pattern 13 is boiled variously, and is changed, and thickness h of silicon-oxide layer 14b by SOG changes, and the relation is prepared beforehand Since the thickness t1 and t2 of the silicon-oxide layers 14a and 14c by CVD is simultaneously regularity, it is almost equal. [of the change of thickness h of silicon-oxide layer 14b and the change of thickness H of the layer insulation layer 14 by SOG] H-h=t1+t2= regularity.

[0026] In the experiment which this invention person conducted, three kinds of material was used as SOG. The property shows the almost same inclination to these three kinds of material. The silicon-oxide thickness h by SOG increases to a linear mostly at first, and shows the inclination which weakens a upward tendency soon and is saturated as the width of face W of the wiring layer 13 increases. In the graph shown in drawing 2 , when the wiring width of face W is 50 micrometers or more, the silicon-oxide thickness h by SOG which collects on it becomes almost fixed. In addition, in the sample used for this graph, the silicon-oxide stratification conditions by SOG were chosen so that the silicon-oxide layer by SOG might become about 500nm in thickness on a flat (whole surface) electrode layer.

[0027] The submicron wiring with many patterns with a width of face of 2-3 micrometers of wiring in recent years is not rare at most, either. Considering this situation, it can be said that the width of face of the dummy wiring in an isolated field is more than the double precision of the typical wiring width of face in a high density field.

[0028] It returns to drawing 1 and the process of Step S2 is performed following Step S1. A layer insulation layer is formed in the 1st field which is a wiring high density field on a semiconductor substrate on condition that predetermined, and the thickness is measured. The wiring in a high density field has for example, the minimum wiring width of face, and includes many circuit patterns arranged at an interval equivalent to the minimum wiring width of face. In addition, a dummy circuit pattern is formed in the dead air space during wiring if needed. As for the wiring in this high density field, it is desirable to consider as the same pattern as wiring of the high density field of the actually created semiconductor device.

[0029] Drawing of step S2 right-hand side shows roughly the structure on the semiconductor substrate formed in this process. It crowds on the ground insulating layer 11, a circuit pattern 12 is formed, and the layer insulation layer 14 is formed on it. The height H1 from the front face of the layer insulation layer 14 to circuit pattern 12 front face is measured. In addition, as shown in drawing 2 , when forming a layer insulation layer by the laminated structure, you may measure silicon-oxide layer thickness h by the layer thickness from which thickness changes with ground configurations, for example, SOG.

[0030] Drawing 3 (A) shows the example of the circuit pattern in a high density field. In the high density field, dummy wiring is arranged so that the dead air space which has the width of face more than fixed may not be generated.

[0031] Drawing 3 (B) shows roughly the composition of the layer insulation layer in a high density field. The lower layer wiring 12 which crowded on the ground insulating-layer 11 front face is formed, and the layer insulation layer 14 is formed on it. The layer insulation layer 14 shows the composition which sandwiched silicon-oxide layer 14b by SOG in the silicon-oxide layers 14a and 14c by CVD.

[0032] The thickness H1 of the layer insulation layer 14 formed on lower layer wiring 12 front face has the thickness h1 of silicon-oxide layer 14b by SOG, a fixed relation, and H1-h1= regularity. Therefore, even if it uses the thickness H1 of the whole layer insulation layer as a parameter, you may use the silicon-oxide layer thickness h1 by SOG.

[0033] In Step S3, based on the relation asked at Step S1, it asks for the width of face of the lower layer dummy wiring in an isolated field so that the layer insulation layer thickness for which it asked at Step S2, and the layer insulation layer thickness in an isolated field may be in agreement. That is, as shown in the graph on the right-hand side of drawing, the width of face W of the dummy wiring in an isolated field is determined so that the layer insulation layer thickness H1 for which it asked at Step S2, and the layer insulation layer thickness in an isolated field may become equal.

[0034] As shown in drawing 2 , when a layer insulation layer is the structure which sandwiched the silicon-oxide layer by SOG in the silicon-oxide layer by CVD, you may choose the width of face of dummy wiring so that silicon-oxide layer thickness h by SOG may be on the dummy wiring in a high density field top and an isolated field and may become almost the same. For example, when the silicon-oxide layer thickness by SOG in a high density field is 200nm, the width of face of the dummy wiring in an isolated field is set to about 8-9 micrometers.
[0035] The ground front face of wiring does not need to be the same level strictly. Sufficient precision should just be guaranteed in phot lithography.
[0036] If such conditions are chosen, in an isolated field, the surface level of a layer insulation layer can be adjusted to the bottom of the upper wiring almost identically only by arranging one dummy wiring.
[0037] Drawing 3 (C) shows roughly the relation between the upper wiring in an isolated field, and the lower layer dummy wiring arranged under it. If it is going to form the silicon-oxide layer by SOG of desired thickness in the bottom of the upper wiring 16, the width of face of the pattern of lower layer dummy wiring will presuppose that it is W1 need. The upper wiring 16 and the lower layer dummy wiring 13 which have such a relation serve as a configuration by which the upper wiring 16 is arranged along the center of the cross direction of the lower layer dummy wiring 13 as shown in drawing.
[0038] In addition, when other patterns exist in the field of the lower layer dummy wiring 13, it is good to leave the gap (for example, gap of the minimum width of face permitted) of predetermined width of face to the circumference of other patterns, as a drawing destructive line shows, and to form lower layer dummy wiring.
[0039] In step S4, while forming lower layer wiring in the 1st field which is a field where wiring crowded, the lower layer dummy wiring which has the width of face for which it asked at Step S3 is formed in the 2nd field which is an isolated field in which it is not crowded with wiring. Here, dummy wiring is formed only down the part in which the upper wiring is formed. Therefore, the amount of data for forming dummy wiring can be decreased remarkably.
[0040] In Step S5, the layer insulation layer 14 is formed on a front face including the 1st field and the 2nd field, and the upper wiring 15 and 16 is formed on it.
[0041] Drawing 4 shows roughly the composition of the semiconductor device which has the wiring structure acquired as a result of the process shown in drawing 1 . The right-hand side in drawing is the high density field RA where wiring crowded, and left-hand side is the isolated field RB in which it is not crowded with wiring. In the high density field RA, the lower layer wiring and the dummy wiring 12 which crowded on the ground insulating layer 11 are formed, and the layer insulation layer 14 is formed on it. The layer insulation layer 14 has the laminated structure which sandwiched silicon-oxide layer 14b by SOG in the silicon-oxide layers 14a and 14c by CVD. In a high density field, silicon-oxide layer 14b by SOG on wiring shows the thickness of simultaneously regularity according to wiring width of face, wiring density, etc.

[0042] In an isolated field, the lower layer dummy wiring 13 which had width of face W chosen like **** on the ground insulating layer 11 is formed, and the layer insulation layer 14 is formed on it. The width of face W of the lower layer dummy wiring 13 is chosen so that the thickness as the thickness of silicon-oxide layer 14b by SOG in a high density field with the almost same thickness of silicon-oxide layer 14b by SOG on it may be realized. Therefore, in the lower layer dummy wiring 13 center-section upper part in an isolated field, the layer insulation layer 14 has the almost same level as the layer insulation layer in a high density field.
[0043] The upper wiring 15 and 16 is formed on layer insulation layer 14 front face. Since the upper wiring 15 and 16 is mostly formed in the same level, it can secure a high phot lithography precision.
[0044] The upper wiring 15 and 16 is covered and an insulating layer 18 is formed further. In addition, an insulating layer 18 is used as a layer insulation film if needed, and a multilayer interconnection is formed. For example, what is necessary is to form and double dummy wiring with the 1st layer and the 2nd layer, and just to make it the ground front face of the 3rd-layer wiring serve as the same level mostly, when isolated wiring exists only in the 3rd layer with three-layer wiring structure.
[0045] Drawing 6 shows roughly the composition of the semiconductor device by other examples of this invention. In this example, the lower layer dummy wiring 13 in an isolated field is formed by two or more circuit patterns 13a and 13b and ... Since the dummy circuit patterns 13a and 13b and ... are not what is used for connection of circuit element, they can choose the size, a distribution, etc. freely more.
[0046] For example, a grid-like dummy circuit pattern is formed in the bottom of the field where **** wiring is formed in the upper layer. If the interval and number of a grid are changed, the silicon-oxide layer thickness by SOG which collects upwards can be changed. A dummy circuit pattern is realizable in various configurations, such as the shape not only of the shape of a grid but a loop. The amount of data for dummy wiring can be decreased by limiting the field in which dummy wiring is formed also in this case. In this example, the width of face of a dummy circuit pattern is the distance from the edge of outside dummy wiring to an edge most. The distance is equivalent to the width of face of dummy wiring of the 1st example.
[0047] Although this invention was explained in accordance with the example above, this invention is not restricted to these. for example, various change, improvement, combination, etc. are possible -- this contractor -- obvious -- it will be .
[0048]
[Effect of the Invention] As explained above, according to this invention, the semiconductor device which arranged the surface level of the layer insulation film in a wiring formation field is offered using limited dummy wiring data.

[Translation done.]